ABSTRACT

A semiconductor device includes a differential level converter circuit that receives a first signal and outputs a second signal of greater amplitude. The differential level converter has a first MISFET pair for receiving the first signal, a second MISFET pair for enhancing the withstand voltage of the first MISFET pair, and a third MISFET pair with cross-coupled gates for latching the second signal from output. The film thickness of the gate insulating films of the second and third MISFET pairs is made thicker than that of the first MISFET pair, and the threshold voltages of the first and second MISFET pairs are made smaller than that of the third MISFET pair. This level converter circuit operates at high speed even if there is a large difference in the signal amplitude before and after level conversion.